Delhi Technological University

(Formerly Delhi College of Engineering)

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN MAY 2025 IS DECLARED AS UNDER:-

Master of Technology(VLSI Design & Embedded System), IV-SEMESTER

Result Declaration Date : 14-07-2025

Notification No: 1861

VLS602 : MAJOR PROJECT II

Sr.No	Roll No.	Name of Student	VLS602 12.00	SGPA	TC	Failed Courses
1	23/VLS/01	BRIJ NANDAN SINGH	A	8.00	12	
2	23/VLS/03	SHASHI RANJAN UPADHYAY	O	10.00	12	
3	23/VLS/04	PRAKHAR SAINI	A	8.00	12	
4	23/VLS/05	MOHAMMAD TALHA	A	8.00	12	
5	23/VLS/06	PRAJVI UDAR	A	8.00	12	
6	23/VLS/07	MAYANK CHAUHAN	A	8.00	12	
7	23/VLS/08	AMARTYA ROY	A	8.00	12	
8	23/VLS/09	DEEPTI	A	8.00	12	
9	23/VLS/10	AASTHA SINGH	A	8.00	12	
10	23/VLS/11	GAJJAR JAY UMESH BHAI	A	8.00	12	
11	23/VLS/12	PREETI	A	8.00	12	
12	23/VLS/13	ASMAR HAFEEZ	A	8.00	12	
13	23/VLS/14	TUSHANT VERMA	A	8.00	12	
14	23/VLS/15	AKHILESH VISHWAKARMA	B	6.00	12	
15	23/VLS/16	RAMLAKHAN	A	8.00	12	
16	23/VLS/17	DEVESH SAINI	C	5.00	12	
17	23/VLS/18	KUNCHA AKHILESH KUMAR	A	8.00	12	
18	23/VLS/19	SOUMYAJIT DAS	A+	9.00	12	
19	23/VLS/20	UJJWAL BHARTI	A	8.00	12	
20	23/VLS/21	TVISHA PUSHKAR	A+	9.00	12	

OIC (Results)

Controller of Examination

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21	23/VLS/23	MANISH SINGH	A	8.00	12	
22	23/VLS/24	ADITYA RAYER	A	8.00	12	
23	23/VLS/25	YASHODA PARMAR	A+	9.00	12	

OIC (Results)

Controller of Examination

Note: Any discrepancy in the result in r/o name/roll no/registration/marks/grades/course code/title should be brought to the notice of Controller of Examination/OIC(Results) within 15 days of declaration of result, in the prescribed proforma.