Delhi Technological University

(Formerly Delhi College of Engineering)

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN NOV 2023 IS DECLARED AS UNDER:-

Master of Technology(VLSI Design & Embedded System), III-SEMESTER

Result Declaration Date : ...   **Notification No: 1652**

OIC (Results)   **Controller of Examination**

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Master of Technology(VLSI Design & Embedded System), III-SEMESTER

Result Declaration Date : 02-02-2024   **Notification No: 1652**

VLS601 : MAJOR PROJECT I

Sr.No	Roll No.	Name of Student	VLS601 3.00	SGPA	TC	Failed Courses
1	2K22/VLS/01	ANKIT RAJ	A	8	3	
2	2K22/VLS/02	BHARGAV SINGH	A	8	3	
3	2K22/VLS/03	BHUVNESH SINGH	O	10	3	
4	2K22/VLS/04	DEAVERCHIT SINGH BAGHEL	A+	9	3	
5	2K22/VLS/05	FARHEEN SAFDAR	A+	9	3	
6	2K22/VLS/06	KUNAL RUPRAJ JAGTAP	A+	9	3	
7	2K22/VLS/07	MAYANK KAUSHIK	A	8	3	
8	2K22/VLS/08	NAKKA SRI KRISHNA CHAITANYA	O	10	3	
9	2K22/VLS/09	NISHANT SHARMA	A	8	3	
10	2K22/VLS/11	RICHA DUBEY	A	8	3	
11	2K22/VLS/12	RUPESH KUMAR	A+	9	3	
12	2K22/VLS/14	SAGAR GOSAI	O	10	3	
13	2K22/VLS/15	SHALU KESHARI	B+	7	3	
14	2K22/VLS/16	SHIV SHANKAR YADAV	O	10	3	
15	2K22/VLS/17	SHUBHAM AGGARWAL	A	8	3	
16	2K22/VLS/18	SHUBHAM GUPTA	A+	9	3	
17	2K22/VLS/19	SUNRIKA	A+	9	3	
18	2K22/VLS/20	SURAJ GUPTA	A	8	3	
19	2K22/VLS/21	SURAJ KUMAR	O	10	3	
20	2K22/VLS/22	TARUN GUPTA	O	10	3	
21	2K22/VLS/23	VIPIN KUMAR SHARMA	A+	9	3	

OIC (Results)

Controller of Examination

Note: Any discrepancy in the result in r/o name/roll no/registration/marks/grades/course code/title should be brought to the notice of Controller of Examination/OIC(Results) within 15 days of declaration of result in the prescribed proforma.

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VLS601 : MAJOR PROJECT I   VLS6207 : Selected topics in VLSI   VLS6401 : Mixed Signal Design

Sr.No	Roll No.	Name of Student	VLS601	VLS6207	VLS6401	SGPA	TC	Failed Courses
			3.00	2.00	4.00			
22	2K22/VLS/10	RAVINDER KAUR	A+	A	A+	8.78	9	

OIC (Results)

Controller of Examination